Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A**
2. **N.A**
3. **B**
4. **N.B**
5. **C**
6. **N.C**
7. **VSS**
8. **N.D**
9. **D**
10. **N.E**
11. **E**
12. **N.F**
13. **F**
14. **VDD**

**.042”**

**.043”**

**13 14 1**

**8 7**

**6**

**5**

**4**

**3**

**2**

**9**

**10**

**11**

**12**

**CD**

**4069UB**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VDD**

**Mask Ref: CD4069UB**

**APPROVED BY: DK DIE SIZE .042” X .043” DATE: 8/25/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .024” P/N: CD4069UBH**

**DG 10.1.2**

#### Rev B, 7/19/02